What is claimed is:

1. A semiconductor integrated device, comprising:

a first circuit unit to which electric power is supplied from a first power supply wiring and a second power supply wiring;

a second circuit unit to which electric power is supplied from a third power supply wiring and a fourth power supply wiring;

a first interface circuit unit formed in the first circuit unit; and

a second interface circuit unit formed in the second circuit unit, the second interface circuit unit being configured to perform any of inputting and outputting a signal to and from the first interface circuit unit,

wherein the second power supply wiring is coupled through at least a protection circuit configured to be conductive at a given voltage or above, to the fourth power supply wiring at a node.

2. A semiconductor integrated device, comprising:

a first circuit unit to which electric power is supplied from a first power supply wiring and a second power supply wiring;

a second circuit unit to which electric power is supplied from a third power supply wiring and a fourth power supply wiring;

a first interface circuit unit formed in the first circuit unit; and

a second interface circuit unit formed in the second circuit unit, the second interface circuit unit being configured to perform any of inputting and outputting a signal to and from the first interface circuit unit,

wherein the second power supply wiring is coupled to the fourth power supply wiring at a node.

3. The semiconductor integrated device according to claim 1, wherein the second interface circuit unit is placed in the vicinity of the first interface circuit unit.

4. The semiconductor integrated device according to claim 2, wherein the second interface circuit unit is placed in the vicinity of the first interface circuit unit.

5. The semiconductor integrated device according to claim 1, wherein the first interface circuit unit and the second interface circuit unit are placed at a boundary between the first circuit unit and the second circuit unit.

6. The semiconductor integrated device according to claim 5, wherein the first interface circuit unit is an interface circuit unit in a first internal circuit unit and the second interface circuit unit is an interface circuit unit in a second circuit unit, and

the first internal circuit unit has a larger number of elements than the second internal circuit

7. The semiconductor integrated device according to claim 5, wherein the first interface circuit unit is an interface circuit unit in a first internal circuit unit and the second interface circuit unit is an interface circuit unit in a second circuit unit, and

the first internal circuit unit has a larger chip area than the second internal circuit

8. The semiconductor integrated device according to claim 1, wherein the second interface circuit unit is coupled to the fourth wiring in the vicinity of a node for the second wiring and the fourth wiring.

9. The semiconductor integrated device according to claim 8, wherein the first interface circuit unit is coupled to the second wiring in the vicinity of the node for the second wiring and the fourth wiring.

10. The semiconductor integrated device according to claim 1,

wherein an external connection pad is coupled to the fourth wiring in the vicinity of a node for the second wiring and the fourth wiring.

11. The semiconductor integrated device according to claim 1,

further comprising an external connection pad coupled to the fourth wiring, and

wherein node for the external connection pad and the fourth wiring is located between a node for the second interface circuit unit and the fourth wiring and a node for the second wiring and the fourth wiring.

12. The semiconductor integrated device according to claim

1,

wherein the first power supply wiring is coupled to the second wiring through a second protection circuit configured to be conductive at a given voltage or above in the vicinity of a node for the second wiring and the fourth wiring.

13. The semiconductor integrated device according to claim 1,

wherein the first power supply wiring is coupled to the second wiring through a second protection circuit configured to be conductive at a given voltage or above, and

a node for the first power supply wiring and the second wiring is located between a node for the first interface circuit unit and the second wiring and a node for the second wiring and the fourth wiring.

14. The semiconductor integrated device according to claim 1,

wherein an external connection pad coupled to the second ground wiring, and

the first power supply wiring is coupled to the second ground wiring through a third protection circuit configured to be conductive at a given voltage or above, and

a node for the third protection circuit and the fourth wiring is located between a node for the second interface circuit unit and the external connection pad.

15. The semiconductor integrated device according to claim 14,

wherein the node for the second interface circuit unit and the fourth wiring is located between the node for the second wiring and the fourth wiring and the node for the fourth wiring and the external connection pad.

16. The semiconductor integrated device according to claim 1,

wherein the first power supply wiring is coupled to the second wiring through a second protection circuit configured to be conductive at a given voltage or above, and

the second power supply wiring is coupled to the fourth wiring through a third protection circuit configured to be conductive at a given voltage or above.

17. The semiconductor integrated device according to claim 1,

wherein each of the first interface circuit unit and the second interface circuit unit comprises a clamp element configured to protect a gate for receiving an input signal.

18. The semiconductor integrated device according to claim 12,

wherein the second wiring is coupled to the first power supply wiring through the protection circuit in a position between a node for the first interface circuit unit and the first power supply wiring, and, an external connection pad of the first power supply wiring.

19. The semiconductor integrated device according to claim

11,

wherein the second protection circuit coupled between the first power supply wiring and the second wiring and the protection circuit coupled between the second wiring and the fourth wiring are formed in a single cell.

20. The semiconductor integrated device according to claim 14,

wherein a node for the third protection circuit and the first power supply wiring is located between a node for the first interface circuit unit and the first power supply wiring, and, an external connection pad of the first power supply wiring.

21. The semiconductor integrated device according to claim 11,

wherein the second protection circuit coupled between the first power supply wiring and the fourth wiring and the protection circuit coupled between the second wiring and the fourth wiring are formed in a single cell.

22. The semiconductor integrated device according to claim 1,

wherein wiring delay between the first interface circuit unit and the second interface circuit is designed to be equal to or less than a given value.

23. An apparatus for designing a semiconductor integrated device, comprising the steps of:

specifying a first interface circuit unit to be formed

in a first circuit unit to which electric power is supplied from first power supply wiring;

specifying a second interface circuit unit to be formed in a second circuit unit to which electric power is supplied from second power supply wiring, the second interface circuit unit configured to input and/or output a signal to and from the first interface circuit unit; and

arranging the first interface circuit unit and the second interface circuit unit closely to each other in accordance with a predetermined placement rule.

24. An apparatus for designing a semiconductor integrated device, comprising the steps of:

specifying a first interface circuit unit to be formed in a first circuit unit to which electric power is supplied from first power supply wiring;

specifying a second interface circuit unit to be formed in a second circuit unit to which electric power is supplied from second power supply wiring; and

performing wiring design so as to reduce wiring delay between the first interface circuit unit and the second interface circuit unit in accordance with a predetermined placement rule.

25. The apparatus for designing a semiconductor integrated device according to claim 23,

wherein the step of specifying the first interface circuit unit includes the steps of:

modifying connection information so as to short circuit a first element having a connection terminal coupled to the

first power supply wiring;

modifying the connection information so as to short circuit a second element having a connection terminal coupled to the second power supply wiring;

providing different texts respectively to the first power supply wiring and the second power supply wiring; and

specifying a node where terminals provided with the different texts are short circuited.

26. The apparatus for designing a semiconductor integrated device according to claim 23,

wherein the step of specifying the first interface circuit unit includes the steps of:

obtaining a first cell for which connection information is modified so as to short circuit a first element having a connection terminal coupled to the first power supply wiring and replacing the first element with the first cell;

obtaining a second cell for which the connection information is modified so as to short circuit a second element having a connection terminal coupled to the second power supply wiring and replacing the second element with the second cell;

providing different names respectively to the first power supply wiring and the second power supply wiring; and

specifying a node where terminals provided with the different names are short circuited.

27. An apparatus for designing a semiconductor integrated device comprising the steps of:

modifying connection information so as to short circuit

a first element having a connection terminal coupled to first power supply wiring;

modifying the connection information so as to short circuit a second element having a connection terminal coupled to the second power supply wiring;

providing different names respectively to different power pads in the first power supply wiring and the second power supply wiring;

specifying a node where terminals provided with the different names are short circuited; and

performing predetermined element modification concerning the specified node.

28. An apparatus for designing a semiconductor integrated device, comprising the steps of:

obtaining a first cell for which connection information is modified so as to short circuit a first element having a connection terminal coupled to first power supply wiring and replacing the first element with the first cell;

obtaining a second cell for which the connection information is modified so as to short circuit an element having a connection terminal coupled to the second power supply wiring and replacing the second element with the second cell;

providing different names respectively to the first power supply wiring and the second power supply wiring;

specifying a node where terminals provided with the different names are short circuited; and

performing predetermined element modification concerning the specified node.

29. The apparatus for designing a semiconductor integrated device according to claim 27,

wherein a cell including a gate protection element is added to or replaced for the specified node.

30. The apparatus for designing a semiconductor integrated device according to claim 28,

wherein a cell including a gate protection element is added to or replaced for the specified node.